CLASS 716, DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK

SECTION I - CLASS DEFINITION

GENERAL STATEMENT OF THE CLASS SUBJECT MATTER

This class provides for electrical data processing apparatus and corresponding methods for the following subject matter:

A. Processes or apparatus for sketching, designing, and analyzing circuit components.

B. Processes or apparatus for planning, designing, analyzing, and devising a template used for etching circuit pattern on semiconductor wafers.

SCOPE OF THE CLASS

(1) Note. Processes and apparatus for the use of digital components in various types of digital logic circuitries or active electrical nonlinear circuits or devices are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(2) Note. Processes and apparatus for connections of electrical components on a printed circuit board are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(3) Note. Processes and apparatus for computer-controlled semiconductor fabrication are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(4) Note. Significantly claimed apparatus external to this class, claimed in combination with apparatus under the class definition, which perform data processing circuit design and analysis, are classified in the class appropriate to the external device unless specifically excluded therefrom.

(5) Note. Nominally claimed apparatus external to this class in combination with apparatus under the class definition is classified in this class unless provided for in the appropriate external class.

SECTION II - REFERENCES TO OTHER CLASSES

SEE OR SEARCH CLASS:

204, Chemistry: Electrical and Wave Energy, subclasses 298.01 through 298.39 for coating, forming, or etching apparatus using atomic particles.

250, Radiant Energy, subclasses 491.1 through 492.3 for irradiating object or material and the ion or electron beam irradiation, per se.

257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), appropriate subclasses for detail structure of active solid-state devices.

324, Electricity: Measuring and Testing, appropriate subclasses for measuring and testing of electrical devices, in general, particularly subclasses 210 through 212 for magnetic information storage element testing and subclasses 765 through 769 for testing of a semiconductor device.

326, Electronic Digital Logic Circuitry, appropriate subclasses for the use of digital components in various types of electronic digital logic circuitries; particularly subclass 10 for the redundancy of circuit components or devices; subclasses 37 through 39, 41, and 47 for the use of programmable devices and their layout interconnections; subclass 38 for the details of setting or programming of interconnections in multifunctional or programmable digital logic circuitry; and subclasses 41 and 47 for significant layout or layout interconnections.

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, appropriate subclasses for the use of electrical components in various types of active electrical nonlinear circuits or devices.

340, Communications: Electrical, subclass 825.83 and 825.84 for the use of programmable devices in selective communication.

345, Computer Graphics Processing and Selective Visual Display Systems, appropriate subclasses for creation and manipulation of graphical objects.

361, Electricity: Electrical Systems and Devices, subclasses 760 through 783 for the connections of electrical components on a printed circuit board.

430, Radiation Imagery Chemistry: Process, Composition, or Product Thereof, subclass 5 for radiation masks used in radiation imaging of semiconductor devices.

438, Semiconductor Device Manufacturing: Process, appropriate subclasses for the process of manufacturing semiconductor devices.

700, Data Processing: Generic Control Systems or Specific Applications, subclass 121 for computer-controlled semiconductor fabrication.

702, Data Processing: Measuring, Calibrating, or Testing, appropriate subclasses for data processing testing, in general.

703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, subclasses 14 through 16 for circuit and logic simulation.

706, Data Processing: Artificial Intelligence, appropriate subclasses for data processing utilizing knowledge base, rule base, and neural networks.

708, Electrical Computers: Arithmetic Processing and Calculating, appropriate subclasses for arithmetic processing and calculating computer.

714, Error Detection/Correction and Fault Detection/Recovery, appropriate subclasses for reliability and availability, particularly subclasses 25 through 46 for fault locating, subclass 30 for scan path testing, subclasses 724 through 745 for testing and detecting error/fault in one or more circuit components.

SUBCLASSES

1 CIRCUIT DESIGN:

This subclass is indented under the class definition. Subject matter comprising means or steps for sketching or outlining of layout of circuit components.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, appropriate subclasses for the use of digital components in various types of electronic digital logic circuitries.

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, appropriate subclasses for the use of electrical components in various types of active electrical nonlinear circuits or devices.

2 Optimization (e.g., redundancy, compaction):

This subclass is indented under subclass 1.

Subject matter comprising means or steps for improving the layout of the designed circuit components as far as possible.

(1) Note. Examples of the circuit design improvements are global redundancy or compaction of the designed circuit layout such that preserving the integrity of the original circuit design in compliance with design rule requirements.

SEE OR SEARCH THIS CLASS, SUBCLASS:

8 through 11 , for improving the floorplanning of the layout area of a circuit design.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclass 10 for the redundancy of circuit components or devices.

3 Translation (e.g., conversion, equivalence):

This subclass is indented under subclass 1.

Subject matter comprising means or steps for converting an original circuit design data to a target circuit design data having different circuit components while performing the same function as the original circuit design by utilizing a rule group for the conversion.

(1) Note. Rule group, design rule, or design specification have substantially the same meaning. They refer to a set of regulations which define the acceptable dimensions and electrical characteristics achievable in a fabrication process.

4 Testing or evaluating:

This subclass is indented under subclass 1.

Subject matter comprising means or steps for determining (i.e., evaluating) the performance of the designed circuit components.

SEE OR SEARCH CLASS:

324, Electricity: Measuring and Testing, appropriate subclasses for measuring and testing of electrical devices, in general, and particularly subclasses 210 through 212 for magnetic information storage element testing and subclasses 765 through 769 for testing of a semiconductor device.

702, Data Processing: Measuring, Calibrating, or Testing, appropriate subclasses for data processing testing, in general.

714, Error Detection/Correction and Fault Detection/Recovery, appropriate subclasses for reliability and availability, particularly subclasses 25 through 46 for fault locating, subclass 30 for scan path testing, and subclasses 724 through 745 for testing and detecting error/fault in one or more circuit components.

5 Design verification (e.g., wiring line capacitance, fan-out checking, minimum path width):

This subclass is indented under subclass 4.

Subject matter comprising means or steps for checking and confirming the circuit component s layout for consistency of the functional and logical correctness.

SEE OR SEARCH CLASS:

703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, subclasses 14 through 16 for circuit and logic simulation.

6 Timing analysis (e.g., delay time, path delay, latch timing):

This subclass is indented under subclass 5.

Subject matter wherein the design verification is confirmed based on timing constraints such as delay or latch timing of the circuit components.

7 Partitioning (e.g., function block, ordering constraint):

This subclass is indented under subclass 1.

Subject matter comprising means or steps for dividing the circuit design into a set of smaller subcircuits arranged in a logical hierarchical structure.

8 Floorplanning:

This subclass is indented under subclass 1.

Subject matter comprising means or steps for enabling exact judgment of accommodation feasibility of using circuit block units or cells on a layout area of an LSI or PCB at the initial designing stage.

SEE OR SEARCH THIS CLASS, SUBCLASS:

2, for improvement of the layout of designed circuit components.

7, for determination of the circuits or subcircuits.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclass 41 and 47 for significant layout or layout interconnections.

9 Detailed placement (i.e., iterative improvement):

This subclass is indented under subclass 8.

Subject matter comprising means or steps for refining the position assignment, the size or the shape of the circuit block units or cells, and evaluating repeatedly the position assignment of the block units or cells until all the cells are replaced as efficiently as possible in a refined portion of the floor planned layout of a PCB or an LSI.

SEE OR SEARCH THIS CLASS, SUBCLASS:

2, for optimization of designed circuit components.

10 Constraint-based placement (e.g., critical block assignment, delay limits, wiring capacitance):

This subclass is indented under subclass 8.

Subject matter wherein the arrangement of circuit block units or circuit components must satisfy one or more positional assignment restraints.

11 Layout editor (e.g., updating):

This subclass is indented under subclass 8.

Subject matter comprising means or steps for revising or modifying the circuit layout interactively by utilizing graphical representations such as icons or menus.

SEE OR SEARCH CLASS:
345, Computer Graphics Processing and Selective Visual Display Systems, appropriate subclasses for creation and manipulation of graphical objects.
706, Data Processing: Artificial Intelligence, appropriate subclasses for data processing utilizing knowledge base, rule base, and neural networks.

12 Routing (e.g., routing map, netlisting):
This subclass is indented under subclass 1.
Subject matter comprising means or steps for determining the interconnections or path nets between circuit blocks or circuit components and input/output bonding pads (pins).

(1) Note. Connection of terminals or nets at the periphery of a block to the terminals of another block is called a netlist.

(2) Note. Netlisting or process of generating a netlist is included in this subclass.

SEE OR SEARCH CLASS:
326, Electronic Digital Logic Circuitry, subclass 38 for the details of setting or programming of interconnections in multifunctional or programmable digital logic circuitry.

13 Global routing (e.g., shortest path, dead space, or duplicate trace elimination):
This subclass is indented under subclass 12.
Subject matter comprising means or steps for evaluating or determining the shortest interconnection paths or minimizing the number of channels required for placing the conductor paths between nets.

(1) Note. In global routing, the wiring path capacities in a path net or between plural path routing regions and their relationships are usually modeled as graph or trees.

(2) Note. Procedures for determining the shortest paths may include, for example, Maze routing algorithm, Lee s algorithm, Soukup s algorithm, Hadlock s algorithm, or Steiner tree-based algorithm.

14 Detailed routing (e.g., channel routing, switch box routing):
This subclass is indented under subclass 12.
Subject matter comprising means or steps for determining the wiring route within a specified circuit region.

(1) Note. A detailed router searches and finds the actual geometric layout of a specific circuit region and considers only one region at a time as opposed to global router which considers the entire circuit regions of the layout.

(2) Note. Detailed routing includes channel routing and switch box routing.

15 PCB wiring:
This subclass is indented under subclass 12.
Subject matter including the routing paths or wiring of circuit components on a printed circuit board.

SEE OR SEARCH CLASS:
361, Electricity: Electrical Systems and Devices, subclasses 760 through 783 for the connections of electrical components on a printed circuit board.

16 PLA, PLD, FPGA or MCM:
This subclass is indented under subclass 12.
Subject matter wherein the circuit components are programmable logic arrays or devices, field programmable gate arrays, or multichip modules.

SEE OR SEARCH CLASS:
326, Electronic Digital Logic Circuitry, subclasses 37 through 39 , 41, and 47 for the use of programmable devices and their layout interconnections.
340, Communications: Electrical, subclass 825.83 and 825.84 for the use of programmable devices in selective communication.

17 Programmable integrated circuit (e.g., basic cell, standard cell, macrocell):
This subclass is indented under subclass 1.
Subject matter wherein the designed circuit utilizes a high-level circuit element such as an arithmetic or logical component selectively operable (i.e., programmable component) to

perform a given or required specific combinational function.

SEE OR SEARCH THIS CLASS, SUBCLASS:

16, for the use of programmable device routers.

SEE OR SEARCH CLASS:

257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), appropriate subclasses for the structure of integrated devices, in general.

326, Electronic Digital Logic Circuitry, appropriate subclasses for the use of integrated devices in digital logic circuitries.

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, appropriate subclasses for the use of integrated devices in miscellaneous active electrical nonlinear circuits.

18 Logical circuit synthesizer:

This subclass is indented under subclass 1. Subject matter comprising means or steps for automatically transforming a high-level design (e.g., functional specification or functional-level logic such as Boolean expression, truth table, or standard macro logic) into its hardware implementation.

SEE OR SEARCH THIS CLASS, SUBCLASS:

3, for translation of an original circuit design data to a target circuit design data.

19 DESIGN OF SEMICONDUCTOR MASK:

This subclass is indented under the class definition. Subject matter comprising means or steps for planning or devising a template used for etching circuit pattern on semiconductor wafers.

SEE OR SEARCH CLASS:

257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), appropriate subclasses for detail structure of active solid-state devices.

430, Radiation Imagery Chemistry: Process, or Product Thereof, subclass 5 for radiation masks used in radiation imaging of semiconductor devices.

438, Semiconductor Device Manufacturing: Process, appropriate subclasses for the process of manufacturing semiconductor devices.

700, Data Processing: Generic Control Systems or Specific Applications, subclass 121 for computer-controlled semiconductor fabrication.

20 Mesh generation:

This subclass is indented under subclass 19. Subject matter comprising means or steps for determining or approximating the surface contour of the mask by mathematical model or algorithm such as numerical analysis.

(1) Note. The shape or boundary of the mask is divided or segmented into rectangular, triangular, or polygon grids for approximation, for example, by differential equations algorithm.

21 Pattern exposure:

This subclass is indented under subclass 19. Subject matter including means or steps for tracing or drawing an electronic pattern on a semiconductor wafer or mask with particle beam.

(1) Note. Examples of particle beams are ion beams, electron beams, or e-beams.

SEE OR SEARCH CLASS:

204, Chemistry: Electrical and Wave Energy, subclasses 298.01 through 298.39 for coating, forming, or etching apparatus using atomic particles.

250, Radiant Energy, subclasses 491.1 through 492.3 for irradiating object or material and the ion or electron beam irradiation, per se.

FOREIGN ART COLLECTIONS

The definitions below correspond to abolished subclasses from which these collections were formed. See the Foreign Art Collection schedule of this class for specific correspondences. [Note: The titles and definitions for indented art collections include all the details of the one(s) that are hierarchically superior.]

FOR 489 Circuit DESIGN AND ANALYSIS (364/489):

Foreign art collection for subject matter wherein the components are electrical components interconnected into functional configurations.

FOR 490 Integrated (364/490):
Foreign art collection for subject matter wherein the circuits are a combination of interconnected circuit elements inseparably associated on or within a continuous substrate.

FOR 491 Layout (364/491):
Foreign art collection for subject matter comprising means or steps for designing and analyzing topological arrangement of conductors and components in an integrated circuit.

END